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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,111	10/10/2003	Syotaro Ono	243808US2S	8211
22850	7590	07/19/2005		
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER WILSON, ALLAN R	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/682,111

Applicant(s)

ONO ET AL.

Examiner

Allan R. Wilson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) 8,9,21,22,34,35 and 56-60 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 43-55 is/are allowed.
- 6) ☒ Claim(s) 1-7 10-20 23-33 36-42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6, 7, 10-13, 16, 17, 19, 20, 23-26 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by 6,008,520 to Darwish et al. Darwish teaches, with reference to figure 4, a semiconductor device comprising:

- a first semiconductor layer 111 of a first conductivity type (N-type);

- a second semiconductor layer 116 of a second conductivity type (P-type) formed on a main surface of the first semiconductor layer;

- a third semiconductor layer 112 of the first conductivity type formed in the second layer 116 and electrically isolated from the first layer 111;

- a trench formed to extend from the surface of the third layer and penetrate the third layer and having depth to reach at least a portion lying near the first layer 111 (the trench is not labeled in fig. 4 but is generally that area filled with elements 102/106);

- a first insulating film 106 formed on sidewalls and a bottom portion of the trench;

- a first electrode 102 formed at least partly on the first insulating film in the trench and electrically isolated from the first to third layers; and

a fourth semiconductor layer 402 of the first conductivity type formed near the trench on an interface between the first 111 and second 116 layers and having an impurity concentration higher than that of the first layer (see fig. 5 showing delta layer (402) having a higher concentration than drift region 111);

wherein an impurity concentration profile of the second layer 116 has first and second peaks (note in fig. 4 that region 116 has a P+ peak at both the top and bottom of the region).

Regarding claims 2-4 and 17, Darwish teaches that the second layer 116 has a plurality of peaks (as designated by "P+" in fig. 4) such that a peak is formed at the interface between the second and third layers and the second and fourth layers. Regarding claims 6 and 19, Darwish teaches that the fourth layer 402 is formed near the bottom of the trench. Regarding claims 7 and 20, Darwish teaches that the trench penetrates the first and fourth layers and that the fourth layer is formed on the sidewall of the trench (fig. 4, and see fig. 11D). Regarding claim 10 and 23, Darwish teaches in figure 4 that the interface between the first and second layers 111 and 116 is shallow near the trench and deeper in a peripheral portion (e.g. layer 116 has a deeper portion away from the trench). Regarding claim 11 and 24, Darwish teaches in figure 5 the depths of the layers including the depth of the body region or second layer 116, the delta layer 402 and the depth of the drift region 111. As shown in figures 4 and 5, the depth of the body region is less than 3 μm deep and the bottom of region 116 is not more than 1.2 μm from the bottom of the trench. Regarding claim 12 and 25, Darwish teaches a fifth layer 114 formed adjacent to the third layer 112. With regard to claims 13 and 26, Darwish teaches the first electrode is formed of polysilicon (col. 2, lines 5-6). With regard to claims 16 and 29, Darwish teaches a second

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electrode (not shown, col. 1, lines 66-67) and a third electrode 118 formed on the top surface of the device, over the third and fifth layers and a second insulating film 117.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darwish in view of 2003/0235959 to Lichtenberger et al. Darwish taught the device of claims 1 and 17 but did not expressly disclose that the insulating film thickness was greater at the bottom of the trench than at the sidewalls of the trench. Lichtenberger teaches in figure 4 a vertical DMOS device in which trench insulating film 44 is thicker at the bottom of the trench than at the sides 15. Darwish and Lichtenberger are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Darwish having a thicker insulating film at the bottom of the trench as compared to at the side. The motivation for doing so, as is taught by Lichtenberger, is that such a thicker bottom film minimizes the gate to drain capacitance which is useful for high-frequency applications (para. 0012). Therefore, it would have been obvious to combine Darwish and Lichtenberger to obtain the invention of claims 5 and 18.

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Claims 14, 15, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over '520 to Darwish in view of 2004/0070028 to Azam et al. Darwish taught the device of claims 1 and 17 but did not expressly teach that the gate electrode protruded from the trench or that the part that protrudes comprises a low resistance layer. Azam teaches in figure 1 and 8 a vertical DMOS device having a gate electrode 17 which has a portion 22 that protrudes above a trench. Azam and Darwish are combinable as they are from the same field of endeavor as applicant's invention. At the time of the invention, it would have been obvious to form the device of Darwish having a gate electrode that extends above the trench. The motivation for doing so is that by extending the gate out of the trench, the cross-sectional area is increased and thus the gate resistance is lowered (para. 0011). Azam teaches that the gate electrode is typically made of polysilicon but it may also include silicide (para. 0010). It is considered obvious to form the gate polysilicon and include a top layer of silicide; such structure is well known in the art, the motivation being that silicide has an even lower resistance than polysilicon such that the total gate resistance would be even lower. As such, it is considered obvious to combine Darwish and Azam to obtain claims 14, 15, 27 and 28.

Claims 30, 32, 33, 36-39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over '520 to Darwish in view of 6,600,193 to Darwish. As discussed above, '520 to Darwish teaches the device of claim 30 but it does not expressly disclose that the second layer has at least 40% of the maximum value of the impurity concentration in a region of not less than 60% of that layer. Darwish teaches in the '193 patent, a vertical DMOS device (e.g. fig. 3) wherein the doping profile of the channel or body region 34 has a nearly horizontal cross-section

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which indicates that nearly 100% of the region has at least 40% of the maximum value of impurity concentration (see fig. 13B).

The two patents to Darwish are combinable as they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of '520 to Darwish using the body doping profile as taught in '193. The motivation for doing so is that such doping profile provides higher punch through breakdown voltage (col. 5, lines 40-45). Therefore, it would have been obvious to combine the patents of Darwish to obtain the invention of claims 30, 32, 33, 36-39 and 42.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over '520 and '193 to Darwish as applied to claim 30 above, and further in view of '959 to Lichtenberger et al. Darwish made obvious the device of claim 30 but did not expressly teach that the bottom of the insulating film in the trench was thicker than on the sides. Lichtenberger teaches in figure 4 a vertical DMOS device in which trench insulating film 44 is thicker at the bottom of the trench than at the sides 15. Darwish and Lichtenberger are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device made obvious by Darwish as having a thicker insulating film at the bottom of the trench as compared to at the side. The motivation for doing so, as is taught by Lichtenberger, is that such a thicker bottom film minimizes the gate to drain capacitance which is useful for high-frequency applications (para. 0012). Therefore, it would have been obvious to combine Darwish and Lichtenberger to obtain the invention of claim 31.

Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over '520 and '193 to Darwish as applied to claim 30 above, and further in view of 2004/0070028 to Azam. Darwish made obvious the device of claim 30 but did not teach that the gate electrode extended above the trench. As discussed regarding claims 14 and 15, Azam makes obvious such a gate electrode and provides motivation for its combination with Darwish.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive.

The argument that Darwish '520 does not disclose a fourth semiconductor layer of the first conductivity type formed near the trench on an interface between the first and second semiconductor layer is not persuasive. Darwish '520 clearly illustrates in fig. 4 a fourth semiconductor layer 402 of the first conductivity type (N-type) formed near the trench (filled with 102 and 106) on an interface between the first 111 and second 116 semiconductor layers.

The argument that for "example in Figure 4 of Darwish '520 that delta layer 402 is provided in contact with the side wall of the trench, and is not formed 'near the trench on an interface between the first and second semiconductor layers' as in the claims" is not persuasive. The "in contact with the side wall of the trench" is the same as "near the trench." An layer that is in contact with a trench is by default near the trench. Darwish '520 also clearly illustrates a fourth semiconductor layer 402 on an interface between the first 111 and second 116 semiconductor layers. See drawing below.

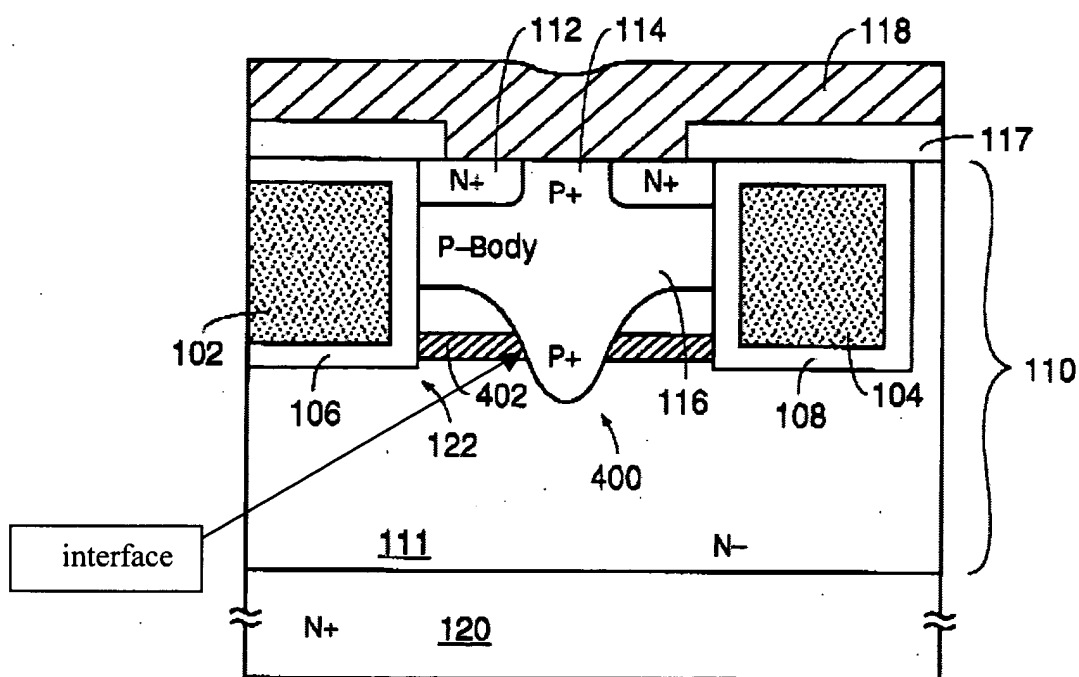


FIG. 4

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The argument that “it is possible to control at high accuracy the length of the channel region generated from the source region 23 to be equal to the length of the trench 24” is not persuasive. Applicant is reminded that intended functional use is given no patentable weight in claims drawn to structure. See *In re Pearson* 181 USPQ 641 and *Ex parte Minks* 169 USPQ 120.

The argument that “Darwish `520 does not does not disclose or suggest the ‘second peak which determines a dose amount of the impurities’” is not persuasive. Darwish `520 illustrates in fig. 4 the second semiconductor layer has first and second peaks P+. The “dose amount of the impurities” is show by the “+” symbol.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a shape similar to a BOX shape) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Allowable Subject Matter

Claims 43-55 are allowed. Withdrawn claims 47 and 48 are rejoined as containing all the limitation of allowed claim 43.

Note: This case has been transferred to a different examiner.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'A. Wilson', with a long horizontal flourish extending to the right.

Allan R. Wilson
Primary Examiner
15 July 2005